Inventor Name Search Result

Your Search was:

Last Name = SHIMASAKI
First Name = SHINYA

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10744788	7134042	150	12/22/2003	FREQUENCY DETECTION CIRCUIT AND DATA PROCESSING APPARATUS	SHIMASAKI, SHINYA
10750970	6826085	150	01/05/2004	NONVOLATILE SEMICONDUCTOR MEMORY DEVICE CAPABLE OF ACCURATELY AND QUICKLY ADJUSTING STEP-UP VOLTAGE	SHIMASAKI, SHINYA
10808240	Not Issued	30	03/25/2004	Pseudo-random number generator	SHIMASAKI, SHINYA
11723206	Not Issued	25	03/16/2007	Data scramble/descramble technique for improving data security within semiconductor device	SHIMASAKI, SHINYA

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Inventor Information for 10/808240

Inventor Name	City	State/Country
SHIMASAKI, SHINYA	KAWASAKI-SHI	JAPAN

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1. **Applications of Low Temperature, AC Superconducting Magnets to Material Processing**
Kasahara, H.; Fujioka, K.; Taniguchi, S.; Ueno, K.; Shimasaki, S.;
Applied Superconductivity, IEEE Transactions on
Volume 16, Issue 2, June 2006 Page(s):1112 - 1115
Digital Object Identifier 10.1109/TASC.2006.871335
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1. **E-BIST: enhanced test-per-clock BIST architecture**
Son, Y.; Chong, J.; Russell, G.;
Computers and Digital Techniques, IEE Proceedings-
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Digital Object Identifier 10.1049/ip-cdt:20020158
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2. **An adjacency-based test pattern generator for low power BIST design**
Girard, P.; Guiller, L.; Landrault, C.; Pravossoudovitch, S.;
Test Symposium, 2000. (ATS 2000). Proceedings of the Ninth Asian
4-6 Dec. 2000 Page(s):459 - 464
Digital Object Identifier 10.1109/ATS.2000.893667
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3. **The power consumption reducing technique of the pseudo-random test pattern generator and the signature analyzer for the built-in self-test**
Murashko, I.; Yarmolik, V.; Puczko, M.;
CAD Systems in Microelectronics, 2003. CADSM 2003. Proceedings of the 7th International Conference. The Experience of Designing and Application of
18-22 Feb. 2003 Page(s):141 - 144
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4. **Seed encoding with LFSRs and cellular automata**
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Design Automation Conference, 2003. Proceedings
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5. **On the use of pseudorandom sequences for high speed resource allocators in superscalar processors**
Srinivasan, S.; John, L.K.;
Computer Design, 1999. (ICCD '99) International Conference on
10-13 Oct. 1999 Page(s):124 - 130
Digital Object Identifier 10.1109/ICCD.1999.808416
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Horan, David; Guinee, Richard;
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28-30 June 2006 Page(s):451 - 456

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7. **Behavioral test benches for digital clock and data recovery circuits using Verilog-A**
Ahmed, S.I.; Orthner, K.; Kwasniewski, T.A.;
Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005
18-21 Sept. 2005 Page(s):297 - 300
Digital Object Identifier 10.1109/CICC.2005.1568664

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8. **High speed testing of a four-bit RSFQ decimation digital filter**
Herr, Q.P.; Gaj, K.; Herr, A.M.; Vukovic, N.; Mancini, C.A.; Bocko, M.F.; Feldman, M.J.;
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Volume 7, Issue 2, Part 3, June 1997 Page(s):2975 - 2978
Digital Object Identifier 10.1109/77.621942

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9. **A Low-Power DC-DC Converter with Digital Spread Spectrum for Reduced EMI**
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18-22 June 2006 Page(s):1 - 7
Digital Object Identifier 10.1109/PESC.2006.1712244

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10. **Modeling and simulation of time domain faults in digital systems**
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On-Line Testing Symposium, 2004. IOLTS 2004. Proceedings. 10th IEEE International
12-14 July 2004 Page(s):5 - 10

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#4	((((pseudo-random <and> clock)<in>metadata))<AND>((linear feedback shift register) <or> lfsr<in>metadata))	10
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#8	((((pseudo-random <and> clock)<in>metadata))<AND>((linear feedback shift register) <or> lfsr<in>metadata))	10
#9	((((pseudo-random <and> clock)<in>metadata))<AND>((linear feedback shift register) <or> lfsr<in>metadata))	10

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